REMARKS

Claims 1-5, 8-16 and 19-31 are pending in the application.

Claims 1-5, 8-16 and 19-31 have been rejected.

No Claims have been amended, and reconsideration is respectfully requested in light of the arguments set forth below.

I. REJECTION UNDER 35 U.S.C. § 101

Claims 1-5, 8-16 and 19-31 are newly rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The rejection is respectfully traversed.

The Office Action asserts these claims "merely disclose steps/components for adding two arguments without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim . . ". Office Action, page 2. This rejection and the underlying reasoning are not well taken for the reasons set forth below.

Independent Claim 1 recites an apparatus. The apparatus clearly defines structure (M adder cells arranged in M rows) operable for performing various functions to produce some concrete and tangible result. These functions include generating at least four conditional carry-out bits, propagating certain carryout bits through pass gates (first pass gate, second pass gate), and outputting two conditional carryout bits to other circuitry. Section 101 clearly contemplates this apparatus or machine as statutory subject matter.

Independent Claim 12 recites a data processor. The data processor clearly defines structure (an instruction pipeline having N stages, at least one stage having an M-bit adder with M adder cells arranges in R rows) operable for performing various functions to produce some concrete and tangible result. These same functions are described in the preceding paragraph. Similarly, section 101 clearly contemplates this structure meeting the statutory requirement.

Independent Claim 23 recites a method (process). Section 101 defines a process as statutory subject matter. The method includes receiving data bits, calculating carryout bits, selecting one bit out of two bits, generating carryout bits, and outputting carryout bits to other circuitry. This method unambiguously produces some concrete and tangible result using a specific method.

Accordingly, Applicant's claims fall within statutory subject matter, and the Applicant respectfully requests withdrawal of the § 101 rejection of Claims 1-5, 8-16 and 19-31.

II. REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Uya (US 4,682,303). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is

found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

In reply to Applicant's prior response, the Office Action now clarifies that the adder cells in Uya that may be the least significant bit adders cells in a row of adder cells may be either the Bit 0, Bit 4, Bit 8, Bit 13, or Bit 19 adder cell. First, Applicant's claims recite that its least significant adder cell receives first and second conditional carryout bits. Since Uya's Bit 0 adder cell does not receive any conditional carryout bits, the Bit 0 adder cannot meet this limitation. Second, Applicant's claims recite that the conditional carryout bits generated by the least significant bit adder of the first row are calculated assuming row carry-out bits of 0 and 1 from a second row of adders preceding the first row. Since Uya's Bit 4 adder cell does not receive any conditional carryout bits from the P1 adder, Uya's Bit 4 adder cell does not meet this limitation. This only leaves Uya's Bit 8, Bit 13 or Bit 19 adder cells which might meet the "least significant adder cell" in the first row recited limitation.

Applicant's claims also recite that the second adder cell in the first row receives the conditional carryout bits from the least significant adder cell and generates its two conditional carryout bits by propagating the received conditional carryout bits through a first pass gate and a second pass gate when the first input data bit (A) and the second input data bit (B) are unequal. Uya's Bit 9, Bit 14 or Bit 20 adder cells are the only adder cells that could possibly meet the "second adder cell" limitation (in the same row as the least significant adder cell) in the claims. Though not expressly disclosed, Applicant can only assume that Uya's Bit 9, Bit 14 or Bit 20 adders would be

equivalent in structure to the Bit 5 adder cell shown Figures 3 or 4. It is clear from Uya's Figure 3 that the Bit 5 adder in the row does not propagate the received carryout bits (C5) through a first pass gate and a second pass gate when the first data bit A_5 and the second data bit B_5 are unequal to generate the next carryout bits (C6). Uya, Figure 3.

The Office Action further argues that Uya's logic gates 54-55 meet Applicant's first and second pass gates. In order to be consistent with the Office Action's prior interpretation of the "least significant adder cell", Uya's C26 carryout bits are propagated based on carryout bits C19 from the adder P4 -- not based on whether two data bits A and B in a second adder are unequal, and not using pass gates. The elements in Uya described in the Office Action as meeting the specific claim elements recited in Applicant's claims simply do not meet the claimed elements as they are arranged, and the Office Action's reasoning and interpretation is inconsistent with the disclosure and teachings of Uya.

Applicant notes that the Office Action identifies carryout bits C8 as Applicant's first and second carryout bits generated from the first least significant adder cell and which are provided to the second adder cell, and also identifies the C19 carryout bits as Applicant's carryout bits received by the second adder cell. The Office Action also identifies carryout bits C25 as Applicant's carryout bits from the second adder cell that are propagated through pass gates. This is clearly erroneous.

Therefore, and in either scenario of interpretations, Uya fails to disclose each and every element as they are arranged in Applicant's claims.

As noted in the Applicant's specification, in one embodiment, the time critical data paths through the adder cells in each row are the dual carry paths. See, Specification, page 26, lines 16-20. Applicant utilizes pass gates (or switches) to decrease the delay in these paths. Uya does not disclose the recited elements/features in Applicant's independent claims (as amended).

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-5, 8-16 and 19-31.

III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

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